CLAIMS

1. A method to equalize signals transmitted on a line, the method comprising the following phases:

applying in series with said line, an analogical adaptive filter having a working frequency band, a pole, and a zero, the pole and zero each having a position in said working frequency band that is variable in response to attenuation of said line;

applying to an output of said filter a retroaction circuit able to vary the position of said pole and said zero;

setting said pole and zero in correspondence to a prefixed frequency of said working frequency band;

moving the position of said pole toward high frequencies at the increasing of said attenuation of said line; and

moving the position of said zero toward low frequencies at the increasing of said attenuation of said line.

2. A method in accordance to the claim 1, further comprising:

positioning a first couple of poles/zeros of said analogical adaptive filter to a first prefixed frequency in said working frequency band;

positioning a second couple of poles/zeros of said analogical adaptive filter to a second prefixed frequency in said working frequency band, wherein said first prefixed frequency is greater than said second prefixed frequency

spacing said first and second prefixed frequency in a logarithmic way in said working frequency band;

moving the poles of said first and second couple of poles/zeros toward the high frequencies at the increasing of said attenuation of said line; and

moving the zero of said first and second couple of poles/zeros toward the low frequencies to the increasing of said attenuation of said line.

3. A method in accordance to the claim 2 moving a position of the first couple of pole/zero and in succession a position of the second couple of pole/zero at the increasing of said attenuation of said line.

4. A method in accordance to the claim 1 wherein said pole and zero are placed in a frequencies plane in correspondence of said prefixed frequency in order to equalize the attenuation of said line when said line has null attenuation.

5. A method in accordance to the claim 1 wherein said pole and said zero are moved approximately 30% compared to their initial position.

6. A method in accordance to the claim 1 wherein at the increasing of said attenuation of said line after the moving phases of the position of said pole and of said zero comprises the phase of increasing a continuous gain of said adaptive filter.

7. A method in accordance to the claim 1 wherein said retroaction circuit includes a compensation circuit that compensates for thermal and constructive variations.

8. An equalizer circuit of signals transmitted on a line having an attenuation comprising:

an analogical adaptive filter coupled in series with said line and including plural transconductance filters each having a respective bias current, a pole, and a zero, the pole and zero each having a respective position in frequency in a working band that is variable in response to said respective bias current; and

a retroaction circuit coupled to an output of said adaptive filter and able to vary said respective bias currents, each bias current varying at a varying of said attenuation of said line; wherein each bias current of said plural transconductance filters has a prefixed value and is made to vary at an increase of said attenuation so that said pole of the bias current is moved toward high frequencies of said said zero is moved toward low frequencies.

9. An equalizer circuit in accordance to the claim 8 wherein:

said adaptative analogical filter includes four transconductance filters each having a bias current each with two couples of poles and of zeros, the poles and zeros each having a position in frequency in a working band that is variable in response to said bias current;

said two couples of poles/zeros are placed having a logarithmic spacing in said working frequency band;

said bias current is made to vary so that said poles are moved toward the high frequencies at the increasing of said attenuation of said line; and

said bias current is made to vary so that said zeros are moved toward the low frequencies at the increasing of said attenuation of said line.

10. An equalizer circuit in accordance to the claim 8, further comprising a bias generating circuit able to modify said bias current in response to temperature variations.

11. An equalizer circuit in accordance to the claim 8 wherein the equalizer circuit is realized in CMOS technology.

12. An equalizer for signals transmitted on a line having an attenuation, the equalizer comprising:

an adaptive filter including:

an input coupled to an input portion of the line;

an output coupled to an output portion of the line;

a first transconductance filter having a bias input at which a first bias current is produced; and

a second transconductance filter having a bias input at which a second bias current is produced;

a line attenuation detector coupled to the output of the adaptive filter and structure to detect attenuation in the line; and

a variable bias generator having an input coupled to the line attenuation detector, a first output coupled to the bias input of the first transconductance filter, and a second output coupled to the bias input of the second transconductance filter, the variable bias generator being structured to vary the first and second bias currents in response to receiving an indication from the line attenuation detector that the attenuation has changed.

13. The equalizer of claim 12 wherein the variable bias generator includes:

an input transistor having an input terminal coupled to the line attenuation detector, a first conduction terminal, and a second conduction terminal coupled to a first reference voltage;

a first current mirror having a first leg coupled to the first conduction terminal of the input transistor and a second leg; and

a second current mirror having a first leg coupled to the second leg of the first current mirror and a second leg coupled to the bias input of the first transconductance filter.

14. The equalizer of claim 13 wherein the variable bias generator includes:

a connecting transistor having an input terminal coupled to a second reference voltage, a first conduction terminal, and a second conduction terminal coupled to the first conduction terminal of the input transistor; and

a third current mirror having a first leg coupled to the first conduction terminal of the connecting transistor and a second leg; and

a fourth current mirror having a first leg coupled to the second leg of the third current mirror and a second leg coupled to the bias input of the second transconductance filter.

15. The equalizer of claim 13 wherein the variable bias generator further includes:

a third current mirror having a first leg that includes the first and second current mirrors and a second leg on which a reference current is produced.

16. The equalizer of claim 15 wherein the variable bias generator includes a bias transistor having an input terminal, a first conduction terminal coupled to the second leg of the third current mirror, and a third conduction terminal coupled to the first reference voltage, the equalizer further comprising:

a bias generator coupled to the input terminal of the bias transistor, the bias generator being structured to compensate the bias current against temperature changes.

17. The equalizer of claim 16 wherein the bias generator includes:

a differential couple having an output; and

a fourth current mirror having a first leg coupled to the output of the differential couple and a second leg coupled to the input terminal of the bias transistor.

18. The equalizer of claim 12, further comprising:

a charge pump having an input connected to the line attenuation detector and an output connected to the variable bias generator; and

a capacitor connected between the output of the charge pump and a reference voltage.

19. The equalizer of claim 12, further comprising:

a comparator having a first input coupled to the output portion of the line, a second input coupled to a voltage reference, and an output coupled to the line attenuation detector.

20. The equalizer of claim 19 wherein the line attenuation detector includes:

a NOR gate having first and second inputs and an output;

a first bistable circuit having a first input coupled to the output of the comparator and to the second input of the NOR gate, a second input coupled to the output of the NOR gate, and an output coupled to the first input of the NOR gate; and

a second bistable circuit having an input coupled to the output of the first bistable circuit and an output coupled to the variable bias generator.